

Features

- Uses PingWei advanced PerfectMOS5 technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g \times R_{DS(on)}$ product(FOM)
- Excellent Low Ciss
- Qualified according to JEDEC criteria

Beneficts

- High robustness and reliability
- Increases maximum current capability
- Low power loss, high power density
- Easy paralleling

Applications

- Synchronous Rectification for AC/DC Quick Charger
- Battery management
- UPS (Uninterruptible Power Supplies)

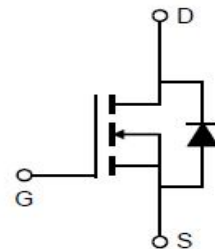
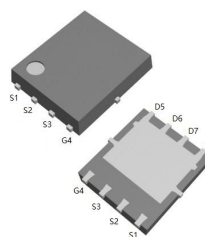


100% DVDS Tested
100% Avalanche Tested

Product Summary

V_{DS}	100V
$R_{DS(on)}@10V$ typ	10mΩ
I_D	40A

DFN3×3



Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
D40N10HS	D40N10HS	DFN3*3	Tape&Reel	13 inches	12mm	5000pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	100	V
Continuous drain current	I_D	77	A
$T_C = 25^\circ\text{C}$ (Silicon limit)		40	
$T_C = 25^\circ\text{C}$ (Package limit)		49	
$T_C = 100^\circ\text{C}$ (Silicon limit)		8	
$T_a = 25^\circ\text{C}$			
Pulsed drain current ($T_C = 25^\circ\text{C}$, $t_p = 100\mu\text{s}$)	$I_{D \text{ pulse}}$	160	A
Avalanche energy, single pulse ($L=0.5\text{mH}$, $V_{ds}=50\text{V}$)	E_{AS}	36	mJ
Gate-Source voltage	V_{GS}	± 20	V
Power dissipation	P_{tot}	125	W
$T_C = 25^\circ\text{C}$		1.4	
$T_a = 25^\circ\text{C}$			
Operating junction and storage temperature	T_j, T_{stg}	-55...+150	$^\circ\text{C}$
Soldering temperature, wave soldering only allowed at leads (1.6mm from case for 10s)	T_{sold}	260	$^\circ\text{C}$

Thermal Resistance

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Thermal resistance, junction – case.	RthJC	-	0.5	1.0	°C/W	-
Thermal resistance, junction - ambient(min. footprint)	RthJA	-	-	92	°C/W	-

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		

Static Characteristic

Drain-source breakdown voltage	BV _{DSS}	100	-	-	V	V _{GS} =0V, I _D =250uA
Gate threshold voltage	V _{GS(th)}	2	-	4	V	V _{DS} =V _{GS} , I _D =250uA
Zero gate voltage drain current	I _{DSS}	-	0.02	1	μA	V _{DS} =100V, V _{GS} =0V T _j =25°C T _j =150°C
Gate-source leakage current	I _{GSS}	-	±10	±100	nA	V _{GS} =±20V, V _{DS} =0V
Drain-source on-state resistance	R _{DS(on)}	-	10.0	12.0	mΩ	V _{GS} =10V, I _D =20A
Transconductance	g _{fs}	-	26	-	S	V _{DS} =5V, I _D =20A

Dynamic Characteristic

Input Capacitance	C _{iss}	-	1251	-	pF	V _{GS} =0V, V _{DS} =50V, f=1MHz
Output Capacitance	C _{oss}	-	434	-		
Reverse Transfer Capacitance	C _{rss}	-	30	-		
Gate Total Charge	Q _G	-	24	-	nC	V _{DS} =80V, I _D =20A , V _{GS} =10V
Gate-Source charge	Q _{gs}	-	7	-		
Gate-Drain charge	Q _{gd}	-	9	-		
Turn-on delay time	t _{d(on)}	-	12	-	ns	V _{GS} =10V, V _{DD} =50V, R _{G_ext} =5Ω, I _D =20A
Rise time	t _r	-	38	-		
Turn-off delay time	t _{d(off)}	-	20	-		
Fall time	t _f	-	6	-		
Gate resistance	R _G	-	1.3	-	Ω	V _{GS} =0V, V _{DS} =0V, f=1MHz

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.88	1.2	V	$V_{GS}=0V, I_{SD}=20A$
Body Diode Continuous Forward Current	I_S	-	-	40	A	$TC = 25^{\circ}C$
Body Diode Pulsed Current	I_S pulse	-	-	160	A	$TC = 25^{\circ}C$
Body Diode Reverse Recovery Time	t_{rr}	-	56	-	ns	$V_R=45V, I_F=5A,$ $dI/dt=100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{rr}	-	139	-	nC	

Typical Performance Characteristics

Fig 1: Output Characteristics

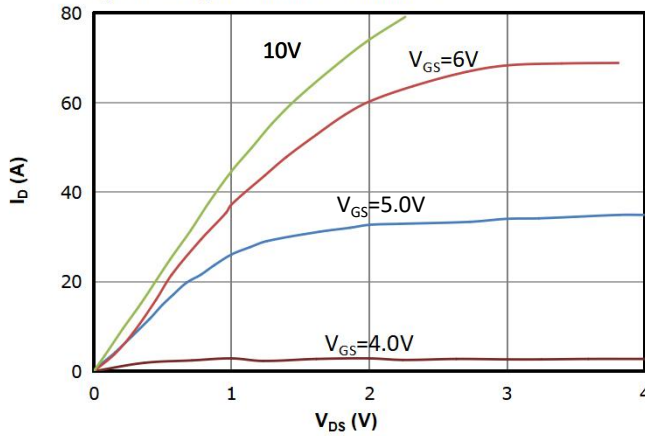


Fig 2: Transfer Characteristics

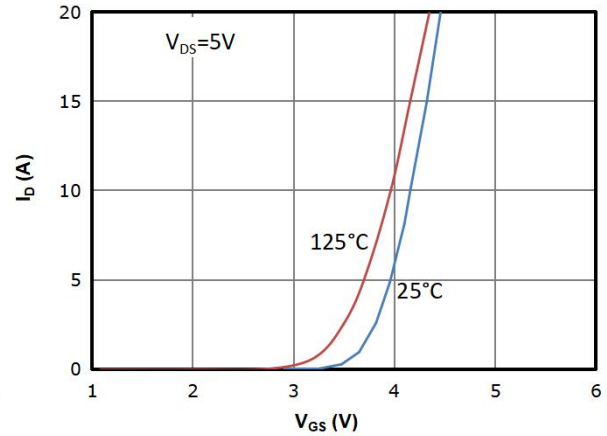


Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

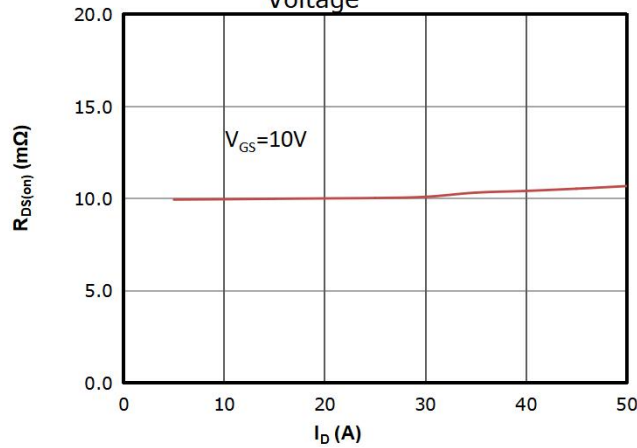


Fig 4: $R_{DS(on)}$ vs Gate Voltage

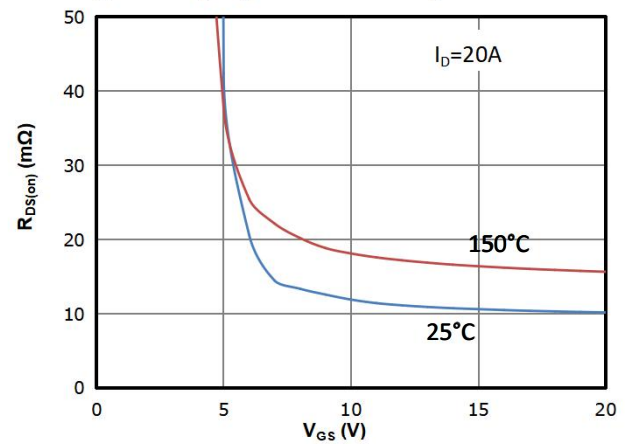


Fig 5: $R_{DS(on)}$ vs. Temperature

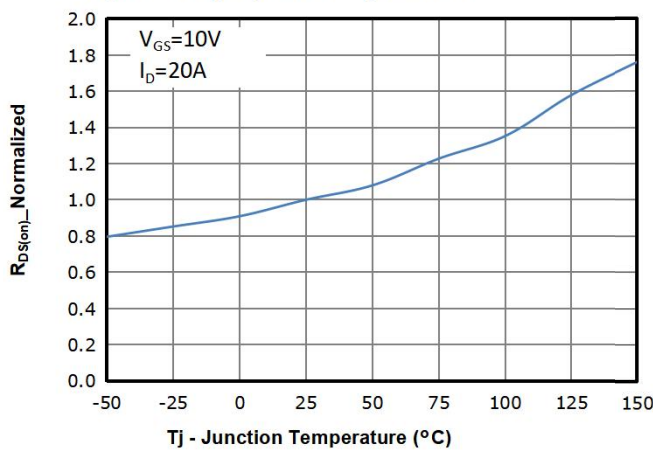


Fig 6: $V_{GS(th)}$ vs. Temperature

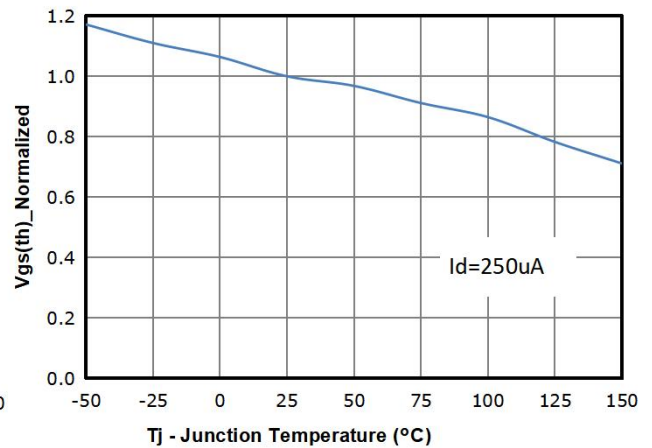


Fig 7: BVdss vs. Temperature

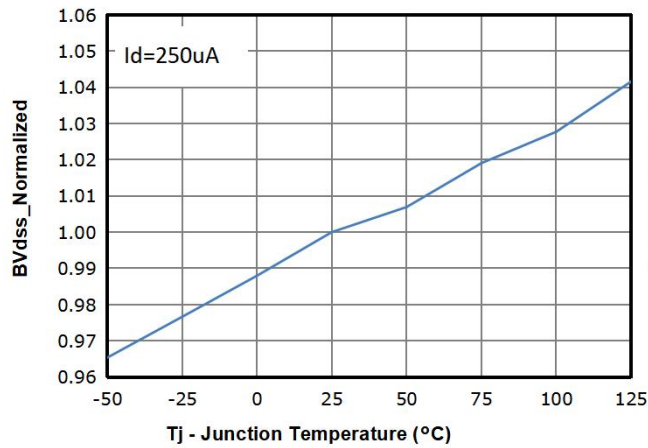


Fig 8: Capacitance Characteristics

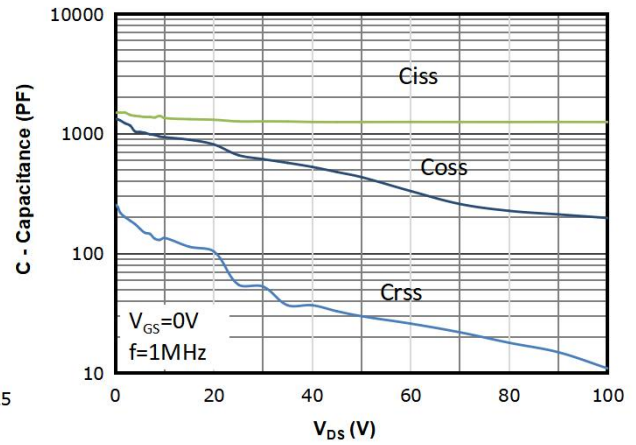


Fig 9: Gate Charge Characteristics

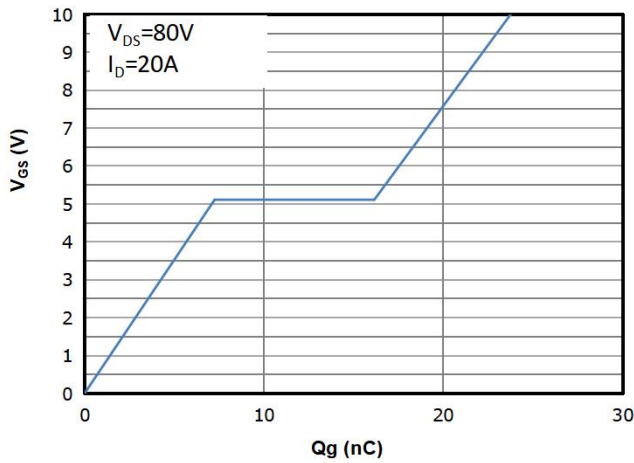


Fig 10: Body-diode Forward Characteristics

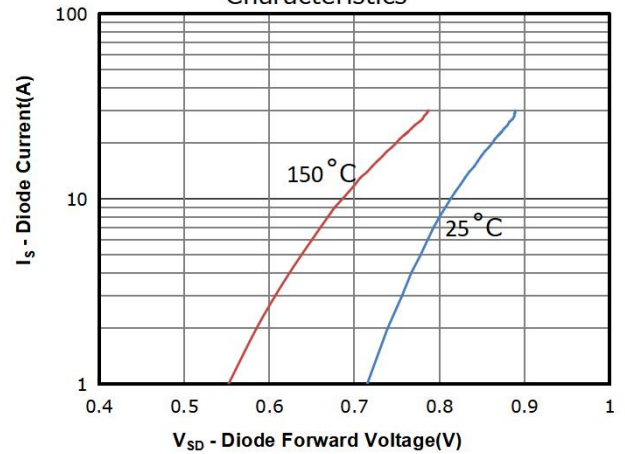


Fig 11: Power Dissipation

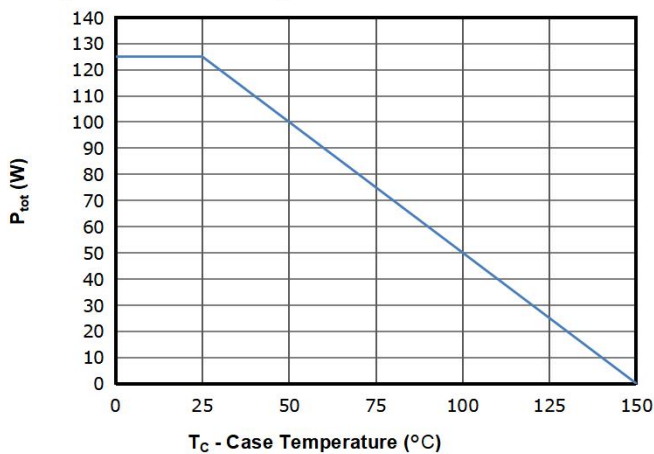


Fig 12: Drain Current Derating

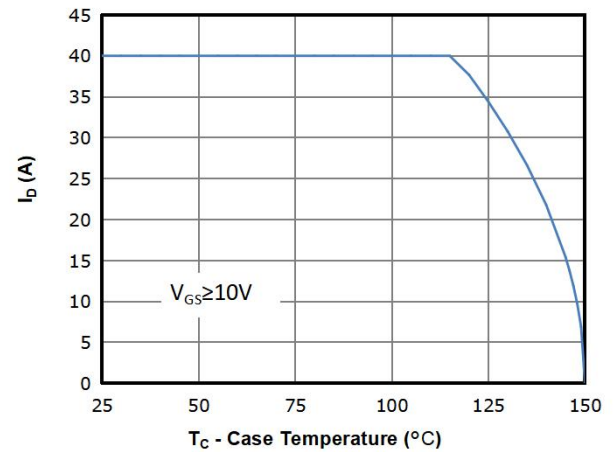


Fig 13: Safe Operating Area

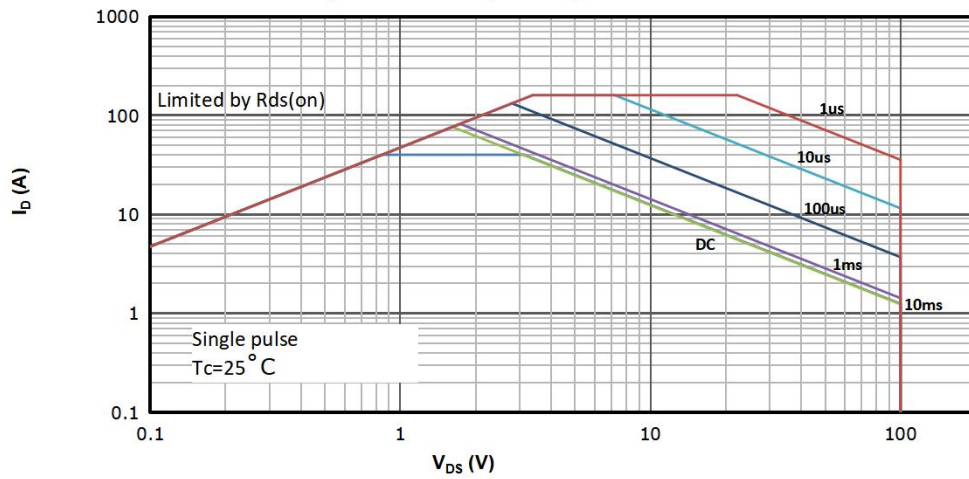
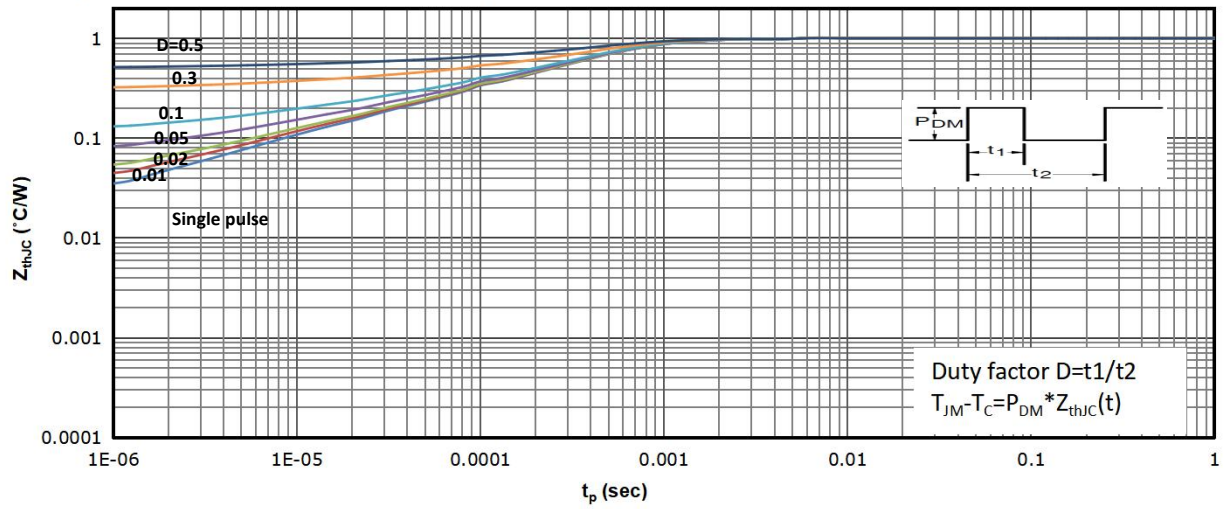
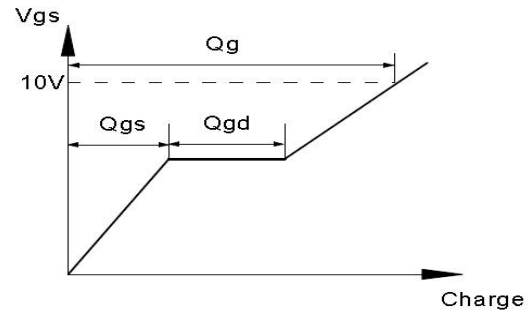
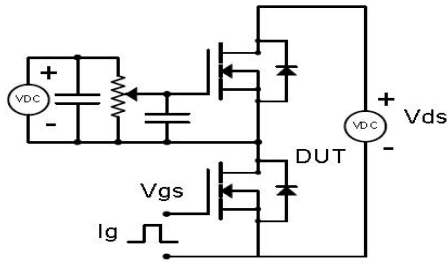


Fig 14: Max. Transient Thermal Impedance

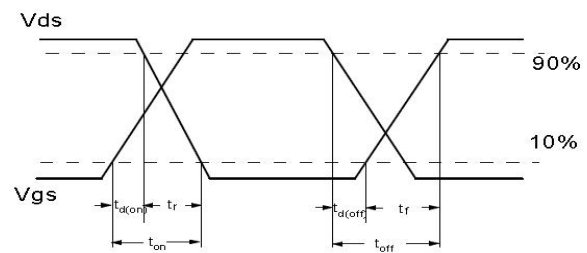
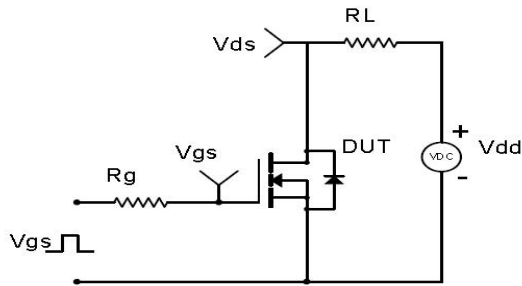


Test Circuit & Waveform

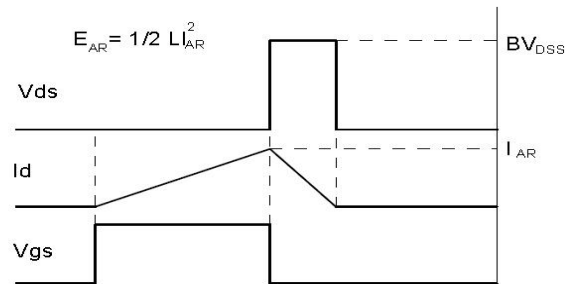
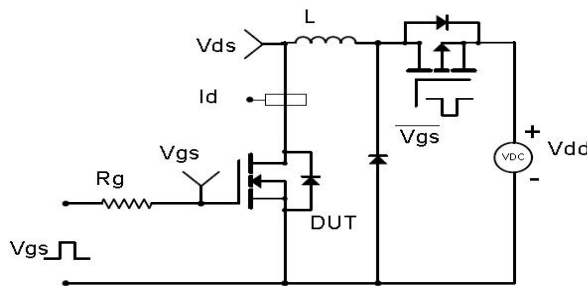
Gate Charge Test Circuit & Waveform



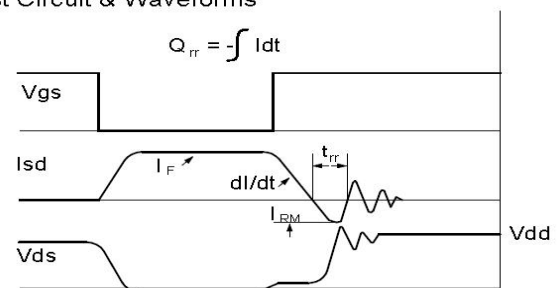
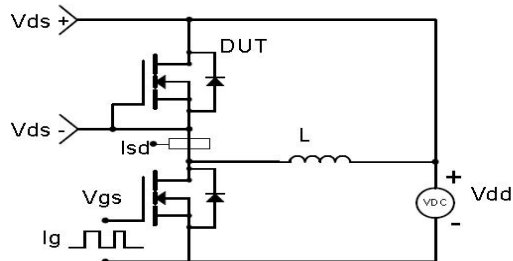
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



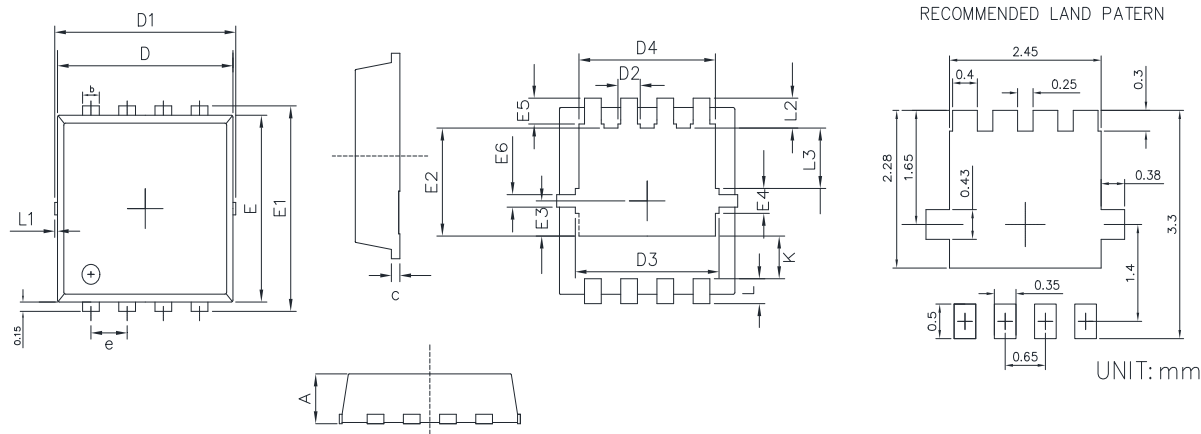
D40N10HS

Perfect MOS5 N-MOSFET 100V, 10mΩ, 40A



重庆平伟实业股份有限公司

Package Outline: DFN3X3



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	1.00	0.028	0.039
b	0.24	0.40	0.009	0.016
c	0.10	0.25	0.004	0.010
D	3.00	3.25	0.118	0.128
D1	3.10	3.50	0.122	0.138
D2	0.30	0.50	0.012	0.020
D3	2.50	2.70	0.098	0.106
D4	2.35	2.55	0.093	0.100
E	2.90	3.10	0.114	0.122
E1	3.15	3.45	0.124	0.136
E2	1.65	1.85	0.065	0.073
E3	0.48	0.68	0.019	0.027
E4	0.23	0.50	0.009	0.020
E5	0.20	0.40	0.008	0.016
E6	0.08	0.25	0.003	0.010
e	0.55	0.75	0.022	0.030
K	0.52	0.82	0.020	0.032
L	0.25	0.55	0.010	0.022
L1	0.00	0.10	0.000	0.004
L2	0.28	0.58	0.011	0.023
L3	0.88	1.08	0.035	0.043



Revision History

Revision	Date	Major changes
1.0	2022/12/30	Release of Formal Version.
1.1	2023/5/16	Update the Tdon/Tr/Tdoff/Tf parameter and Test Condition.

Disclaimer

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